IN THE SPECIFICATION:

Please rewrite paragraph [0057] appearing at Page 13 to read as follows:

--First semiconductor devices 118 such as nFET or pFET are then ~~fabricatED~~ fabricated on the first SOI layer 96 utilizing the techniques described above. Back-end-of the-line processing can be used to form an interconnect structure 150 atop the now fabricated blanket SOI wafer and the above-mentioned processing can be employed in forming the vertical interconnects 75. The resulting structure is shown in FIG. 2C.--